**Dr. Doran K. Wilde**
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## Research Interests

Regular array and systolic architectures, computer arithmetic, processor design, embedded systems, and VLSI circuit design.

## Education

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|---|---|---|
| July 1995 | PhD in Computer Science | Oregon State University |
| June 1994 | Master of Science in Computer Science | Oregon State University |
| April 1978 | Bachelor of Science in Electrical Engineering | Brigham Young University |
| April 1978 | Bachelor of Science in Mathematics | Brigham Young University |

## Employment History

1995 - present Brigham Young University Associate Professor Provo, UT
Teaching in the areas of computer and VLSI design, embedded systems, regular array architectures, and computer arithmetic. Doing research in parallel computation using regular arrays, and computer arithmetic algorithms.

2001 – present Adept Systems Inc. Embedded Systems Orem, UT
Embedded system design of network bridges and routers using state-of-the-art FPGA technology.

2003-2004 Klarquist Sparkman LLP Expert Witness Portland, OR
Testified in federal court in a patent validity and infringement case for plaintiff. Evaluated patent, prior art, patent history, and defendants' expert report. Produced expert reports offering opinion on claim construction, defending validity and showing infringement. Gave deposition and testified to jury in federal court. Jury ruled in favor of plaintiff.

1995-1997 Broadcast International Expert Witness Salt Lake City, UT
Testified in federal court in a firmware copyright infringement suit. Evaluated the evidence, which included EPROMs, assembly code and C code listings, and produced an expert report of my findings. Prepared exhibits and testimony for court. Gave deposition and testified in pretrial hearings. The case settled out of court in terms favorable to Broadcast International.

1992-1995 Oregon State University Research Scientist Corvallis, OR
Conducted research in the compilation of functional languages and the synthesis of regular array architectures. Received a PhD in Computer Science, July 1995.

1992-1994 IRISA Research Scientist Rennes, France
Developed algorithms and software to do computer-aided design of regular array architectures using the ALPHA language. Conducted research in parallel compilers. Developed the polyhedral library which does Boolean operations on general *n*-dimensional polyhedra.

1991-1992 Intel Corporation Expert Witness Sunnyvale, CA
Technical consultant to Intel in the Intel vs AMD litigation of a mask work infringement case. Evaluated the evidence, including deposed documents and layouts of both the Intel 80287 and AMD 80287 math coprocessors. Provided technical opinions, expert reports, and prepared court exhibits and summaries of fact concerning the similarities in the design of the two chips.

1991 Binary Technologies Software Engineer Hillsboro, OR
Developed software to control a printed circuit board tester for an Intel CPU board product. Created a window based test environment and designed a test suite for the product.

1983-1990 NCUBE Corporation MicroArchitect Beaverton, OR
Designed the first and second-generation NCUBE processors. The second processor was a 460,000 CMOS transistor, high performance VLSI processor that included an instruction decoder, cache memory, DRAM controller, 64-bit IEEE 754 standard compliant floating-point execution unit. Wrote high level, and RTL simulation models for this processor.

1978-1983 Intel Corporation VLSI Design Engineer Beaverton, OR
Designed logic for the 43201 microcode sequencer, 43203 I/O processor, 43204 cross-bar interface chip, and 43205 memory interface chip, all of which were VLSI chips in the Intel 432 processor family. Developed new IC design CAD tools and methodologies to manage increasingly complex designs. Pioneered the use of high-level simulation at Intel in 1982. Managed junior engineers. Worked as a college recruiter and interviewed graduates on campus.

1977 Tektronix Research Engineer Beaverton, OR
Worked in Tek Labs and conducted research in using CCD's to do digital signal processing.

## Bibliography

### Refereed conference papers


D.K. Wilde, *A custom processor for use in a parallel computer system*, Proceedings of the IEEE Custom Integrated Circuits Conference, San Diego, California, pp. 10.5/1-10.5/5, May 1989.

R. Andonov, P. Quinton, S. Rajopadhye, and D. Wilde. *A Shift Register Based Implementation of the Knapsack Problem Recurrences*. PARCELLA`94, pages 207-214.

D. Wilde and O. Sie. *Regular Array Synthesis using Alpha*. International Conference on Application Specific Processors. pp. 200-211, Aug 1994.

S. J. Bellis, W. Marnane, D. Wilde, P.J. Fish. *Systolic Arrays for Modified Covariance Spectral Estimation*. EUSIPCO-94, VII European Signal Processing Conference, Sep. 1994.

H. LeVerge, V. VanDongen, D. Wilde. *Loop Nest Synthesis Using the Polyhedral Library*. RenPar`6, June 1994.

P. Quinton, S. Rajopadhye, and D. Wilde. *Derivation of Data Parallel Code from a Functional Program*. 9th International Parallel Processing Symposium (IPPS), pp. 766-772, Santa Barbara, CA. April 1995. IEEE.

P. Quinton, S. Rajopadhye, and D. Wilde. *Deriving Imperative Code from Functional Programs*. 7th Conference on Functional Programming Languages and Computer Architectures (FPCA), pp. 36-44. La Jolla, CA, Jun 1995. ACM.

S. Rajopadhye, and D. Wilde. *The Naive Execution of Affine Recurrence Equations*. International Conference on Application Specific Processors. pp. 1-12, July 1995.

S. Rajopadhye and D. Wilde, *Memory Reuse Analysis in the Polyhedral Model*, Euro-Par`96, Second International Euro-par Conference, Lyon, France, in Lecture Notes in Computer Science, V. 1123, Springer, pp. 389-397, August, 1996.

F. de Dinechin, D. Wilde, S. Rajopadhye, and R. Andonov, *Regular VLSI Array for an Irregular Algorithm*, Irregular`96, Santa Barbara, in Lecture Notes in Computer Science, V. 1117, Springer, pp. 195-200, August, 1996.

Jason Crop, Doran Wilde, *Scheduling Structured Systems.* Europar`99, Fifth International Euro-par Conference, Toulouse, France, in Lecture Notes in Computer Science, V. 1685, pp. 409-412, Sept. 1999.

Jason Crop, Doran Wilde, *Synthesis of Hardware from Affine Recurrence Equations*, International Workshop on Logic Synthesis 1999 (IWLS99), June 1999, Lake Tahoe.

Scott Bowden, Sanjay Rajopadhye, Doran Wilde, *Quadratic Control Signals in Linear Systolic Arrays*, International Conference on Application Specific Systems, Architectures, and Processors, Boston, MA, IEEE Computer Society Press, pp. 268-275, July 2000.

Vincent Loechner, Philippe Clauss, Doran Wilde, Benoît Meister, Rachid Seghir, Gilles Bitran, Julien Léger, *PolyLib: A Library for doing Symbolic Polyhedra Operations*, International Symposium on Symbolic and Algebraic Computation (ISSAC'2002), July, 2002.

Xiaojun Wang, Brent Nelson, Doran Wilde, *Tradeoffs in Designing Floating-Point Division and Square –Root on Virtex FPGAs*, FCCM, April 2003.

Spencer Isaacson, Doran Wilde, *The Task-Resource Matrix: Control for a Distributed Reconfigurable Multi-Processor Hardware RTOS*, International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'04), pp. 130-136, Las Vegas, June 2004.

## Journal papers

J.A Bayliss, J.A. Deetz, S.A. Ogilvie, C. B. Peterson, D. K. Wilde, *The interface processor for the Intel VLSI 432 32-bit computer*, IEEE Journal of Solid-State Circuits, Volume 16, Number 5, pp. 522-530, Oct 1981.

J.A. Bayliss, S.R. Colley, R.H. Kravitz, G.A. McCormick, W.S. Richardson, D.K. Wilde, L.L. Wittmer, *The instruction decoding unit for the VLSI 432 general data processor*, IEEE Journal of Solid-State Circuits, Volume 16, Number 5, pp. 531-537, Oct 1981.

D. Jurasek, W. Richardson, and D. Wilde, *A Multiprocessor Design in Custom VLSI*. VLSI Systems Design, pp. 26-30, June 1986.

R. Andonov, P. Quinton, S. Rajopadhye and D. Wilde. *A shift register based systolic array for the general knapsack problem*, Parallel Processing Letters, Volume 5, Number 2, pp. 251-262, June 1995.

Sanjay Rajopadhye and Doran Wilde, *Memory Reuse Analysis in the Polyhedral Model*, Parallel Processing Letters, Vol. 7 No. 2, pp 203-215, June 1997.

Vincent Loechner, and Doran Wilde, *Parameterized Polyhedra and their Vertices*, in the International Journal of Parallel Programming (IJPP), Volume 25, Number 6, pp. 525-549, Dec 1997.

Fabien Quillere, Sanjay Rajopadhye, Doran Wilde, *Generation of Efficient Nested Loops from Polyhedra*. International Journal of Parallel Processing (IJPP), Volume 28, Number 5, pp. 469-498, Oct 2000.

Doran Wilde, *A Library for Doing Polyhedral Operations*. In the *Journal of Parallel Algorithms and Applications*, Vol. 15, pp. 137-166, 2000.

## Patent Awards

| Patent Number | Date Granted | Title |
|---|---|---|
| 4,243,958 | 6 Jan 1981 | Phase Multiplexed CCD Transversal Filter |
| 4,415,969 | 15 Nov 1983 | Macro Instruction Translator Unit for Use in a MicroProcesso |
| 4,407,016 | 27 Sep 1983 | Microprocessor Providing an Interface between a Peripheral Subsystem and an Object Oriented Data Processor |
| 4,473,880 | 25 Sep 1984 | Arbitration Means for Controlling Access to a Bus Shared by a Number of Modules |
| 4,480,307 | 30 Oct 1984 | Interface for Use between a Memory and Components of a Module Switching Apparatus |
| 4,729,095 | 1 Mar 1988 | Broadcast Instruction for Use in a High Performance Computer System |
| 5,113,523 | 12 May 1992 | High Performance Computer System |
| 5,367,636 | 22 Nov 1994 | Hypercube Processor Network |

## Affiliations

Senior Member IEEE, Tau Beta Pi